## REMARKS

These Remarks are in reply to the Office Action mailed December 11, 2008. Claims 1-16 and 18-21 were pending in the Application prior to the outstanding Office Action. Claims 13-16, 18 and 19 were previously withdrawn. Claim 11 was allowed. Claims 3 and 9 are currently being amended, and new claims 22 and 23 are being added. Thus claims 1-16 and 18-23 remain pending, with claims 1, 3, 9, 11, 22 and 23 being independent. In view of the following remarks, Applicants respectfully request that the outstanding rejections and objections be reconsidered and withdrawn, and that a Notice of Allowance be issued.

### I. Allowable Subject Matter

Applicants thank the Examiner for indicating that independent claim 11 is allowed, and for indicating that objected to dependent claims 3, 10 and 12 would be allowable if rewritten in independent form, including all of the limitations of the base claim and any intervening claims.

### II. Summary of Claim Rejections

Claims 1-2, 4-9 and 21 were rejected under 35 U.S.C. 103(a) for allegedly being unpatentable over U.S. Patent No. 5,875,250 to Kuo et al. (hereafter referred to as "Kuo"), in view of U.S. Patent No. 5,907,482 to Otake (hereinafter referred to as "Otake"). Claim 20 was rejected under 35 U.S.C. 103(a) for allegedly being unpatentable over Kuo in view of Otake and further in view of U.S. Patent No. 6,731,162 to Yeongha et al. (hereinafter referred to as "Yoengha").

### III. Brief Summary of Claimed Embodiments (and Background)

As explained in the Background Section of the present application. At the time the present application was filed, where were a number of problems with existing digital PWM modulation schemes. One of the problems was that audio system implementations were requiring increasing numbers of channels, as explained in paragraph [0007] of the application. As explained in paragraph [0008] of the present application, existing digital PWM amplification systems only had as many channels as can be implemented on a

single chip, e.g., which typically included either two or four channels. As also explained in paragraph [0008], while it may have been possible to provide additional channels on a single chip, this typically was not a practical solution for several reasons, e.g., there may not be enough space on the chip to implement the additional channels, there may not be enough resources (e.g., processor cycles) to process all of the channels on the same chip, and the complexity of the design may have increased dramatically with the additional channels. Still further, even if a few additional channels could be accommodated, such a solution would not address the next generation of system requirements in which still more channels (e.g., 16 channels) were required.

As explained in paragraph [0009] of the present application, at the time of filing the present application, existing digital PWM systems were not implemented across multiple chips because of difficulties that were associated with the interaction of multiple chips, such as the difficulty of synchronization. As explained, in order for a system to provide coherent control of all of the channels in the system, it is necessary to synchronize each of the chips so that they operate essentially as if the system were implemented on a single chip. At the time of filing the present application, no such mechanism existed for digital PWM audio amplification systems.

The various embodiments of the present invention solved one or more of the problems outlined above by enabling the use of multiple digital PWM chips in the same system to provide the additional channels and corresponding capabilities of which were required for many applications. In one embodiment, this is achieved by providing a mechanism through which multiple digital PWM chips can be synchronized, which enables the scaling of systems to provide as many channels as are necessary for any given application.

In a specific embodiment, a plurality of digital audio controllers are implemented on multiple chips, where one of the chips is designated as a master, while the other chips are designated as slaves. A common synchronization line connects all of the chips and is used to transmit synchronization signals from the master to the slaves. When the master chip transmits an appropriate signal, all of the chips detect the signal and simultaneously begin synchronized operation. In this context, "synchronized operation" refers to the chips beginning to operate and doing so in a synchronized manner. It is noted that other

embodiments may also use this mechanism to time-align or phase align the outputs of chips that are already running.

In specific embodiments, the master signals the slaves to begin operation by generating a transition on the shared line, and then repeats the transition at fixed intervals in order to enable the chips to determine whether synchronization is being maintained. The signal may also be maintained for a period of time and sampled and/or filtered to improve reliability. In one embodiment, one or more of the chips can assert a signal on the shared line to indicate that synchronization has been lost. In another embodiment, the chips can communicate over the shared line by transmitting data during periods when synchronization is not being checked. Numerous other features may also be implemented.

## IV. Discussion of Claims

**A.** **Claim 1** is reproduced below for the convenience of the Examiner.

1. A system comprising:
   a plurality of digital pulse width modulation (PWM) controller chips; and
   a synchronization line connected to each of the plurality of chips;
   wherein one of the plurality of chips is a master, and the remainder of the plurality of chips are slaves;
   wherein the master is configured to generate a synchronization signal on the synchronization line; and
   wherein each of the slaves is configured to detect the synchronization signal and, in response to detecting the synchronization signal, to begin generating a corresponding PWM audio output signal which has a known phase relationship to PWM audio output signals generated by the other PWM controller chips.

Claim 1 requires "a plurality of digital pulse width modulation (PWM) controller chips". It was asserted in the Office Action that Kuo teaches this feature of claim 1 because Kuo discloses a single package including at least three separate H-bridge

controllers, each of which are labeled 9 in FIGS. 1A-1G of Kuo. Applicants respectfully disagree with this assertion for at least the following reasons.

One of ordinary skill in the art knows that a "chip" is an integrated circuit manufactured on a semiconductor substrate, which is then typically cut or etched away from the silicon wafer, and then packaged to provide external connections. In other words, the term "chip" is typically used to refer to a packaged semiconductor device. Thus, claim 1 requires a plurality of digital pulse width modulation (PWM) controller chips, where each PWM controller chip is a separate packaged semiconductor device. This is clear from paragraph [0020] of the present application, which specifies that "various embodiments of the invention comprise systems and methods for synchronizing multiple digital audio controller chips (i.e., controllers implemented on different pieces of silicon, so that they cannot be internally synchronized)."

In contrast, in Kuo the three H-bridge controllers are clearly within a "single package", which means the H-bridge controllers are within the same chip. This is clear from FIGS. 1A-1G, where everything within the large block labeled "1" is within a same chip. Accordingly, Kuo does not disclose "a plurality of digital pulse width modulation (PWM) controller chips", as required by claim 1. Further, it is noted that since the H-bridge controllers of Kuo are within the same chip, they will likely not have the same synchronization issues that would occur if each H-bridge controller were within a separate chip.

Further, claim 1 specifies that the plurality of pulse width modulation (PWM) controller chips are **digital** pulse width modulation (PWM) controller chips. In contrast, column 2, lines 64-67 of Kuo state that "[t]he H-bridge controller (9) converts the **analog signal** received from the signal controller (7) to a switching signal as for example by use of a pulse width modulation conversion for use in the class D amplifier operation." Accordingly, Kuo teaches that the H-bridge controllers are analog controllers.

Additionally, claim 1 specifies that "one of the plurality of **chips** is a master, and the remainder of the plurality of **chips** are slaves". It was asserted in the Office Action that Kuo teaches this feature because Kuo at column 3, lines 4-6 specifies that "[i]f

further power is desired, one amplifier channel (2) may be connected as slave to a second amplifier channel (2)". Applicants respectfully disagree with this assertion for at least the following reasons. First, as explained above, all the elements of Kuo are within the same chip, including all three amplifier channels. Accordingly, Kuo is at best saying that one channel can be a slave of another channel with the same chip. Further, Kuo appears to only suggest a slave configuration to increase power. More specifically, to increase power, Kuo appears to configure a half-bridge output to a full-bridge output. Further, in Kuo's supposed master-slave configuration, it appears that the master and slave channels are processing the same audio data, i.e. both the master and slave process the master's audio data.

Claim 1 also requires that "each of the slaves {i.e., each of the digital pulse width modulation (PWM) controller chips that are not the master} is configured to detect the synchronization signal and, in response to detecting the synchronization signal, to begin generating a corresponding PWM audio output signal which has a known phase relationship to PWM audio output signals generated by the other PWM controller chips." It was admitted in the Office Action that Kuo does not teach this feature of claim 1, but it was asserted in the Office Action that Otake teaches this deficiency of Kuo, and that it would have been obvious to modify Kuo based on Otake to provide this feature. Applicants respectfully disagree. Column 3, lines 12-27 of Otake teaches that a master control device (MCD) generates a synchronization signal (RSS) that is received by a slave control device (SCD), which causes the slave control device (SCD) to generate a "triangular-wave voltage whose operation timing and oscillation frequency are the same as those of the single produced by the oscillation circuit 12" of the master control device (MCD). In other words, this portion of Otake explains that the oscillator 22 of the SCD is synchronized with the oscillator 12 of the MCD. However, Otake never teaches that the SCD is configured to "in response to detecting the synchronization signal, **to begin generating a corresponding PWM audio output signal which has a known phase relationship to PWM audio output signals generated by the other PWM controller chips**", as required by claim 1.

**B.** **Claims 2, 4-8 and 20-21** depend from and add additional features to claim 1. Applicants assert that these claims are patentable for at least the reason that they depend from claim 1, as well as for the features that they add.

**C.** **Claim 3**, which has been redrafted to be in independent form, was indicated as being allowable.

**D.** **Claim 9**, which has been redrafted to be in independent form, was indicated as being allowable. **Claims 10 and 12**, which depends from claim 9, are patentable for at least the reason that they depend from claim 9, as well as for the features that they add.

**E.** **Withdrawn claims 13-16 and 18-19** depend from and add additional features to claim 1. Applicants assert that these claims are patentable for at least the reason that they depend from claim 1, as well as for the features that they add.

## V. Conclusion

In light of the above, it is respectfully requested that all outstanding objections and rejections be reconsidered and withdrawn. The Examiner is respectfully requested to telephone the undersigned if he can assist in any way in expediting issuance of a patent.

The Commissioner is authorized to charge the required fees and any underpayment of fees or credit any overpayment to Deposit Account No. 06-1325 for any matter in connection with this reply, including any fee for extension of time, which may be required.

Respectfully submitted,

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